REMARKS

The Office Action mailed November 2, 2009 was received and carefully reviewed.

Claims 1-6 and 13-18 were pending prior to the instant amendment. Claims 7-12 and 19-24 were canceled by a previous reply. Presently, no claims are hereby amended, no claims have been canceled, and no new claims have been added. Consequently, claims 1-6 and 13-18 remain pending in the instant application.

Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Claim Rejections - 35 U.S.C. § 103

Claims 1-4 and 6 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wei et al. (U.S. Patent No.: 5,156,986) (*Wei*, hereinafter) in view of Mori et al. (U.S. Patent No.: 5,243,202) (*Mori*, hereinafter). Claims 5 and 13-18 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Wei* in view of *Mori*, and in further view of Sasaki et al. (U.S. Patent No.: 6,956,236 B1) (*Sasaki*, hereinafter). Applicants traverse the rejections for at least the reasons advanced in detail below.

Independent claims 1-3 and 13-15, and the claims dependent therefrom, are patentably distinguishable over *Wei*, *Mori*, and *Sasaki*, since *Wei*, *Mori*, and *Sasaki*, taken either alone or in combination, fail to disclose, teach, or suggest each and every feature recited in the pending claims. For example, independent claims 1, 3, 13 and 15 are directed to, *inter alia*, a semiconductor element include:

> *...an insulating film that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film...wherein the insulating film is formed to have a laminated-layer structure.* (Emphasis added)

Independent claims 2 and 14 are directed to, *inter alia*, the features of a semiconductor element including:

> *...an insulating film having a thickness of 100 nm or more that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film...wherein the insulating film is formed to have a laminated-layer structure.* (Emphasis added)

Applicants contend that neither *Wei*, *Mori*, nor *Sasaki*, taken either alone or in combination, anticipate or render obvious at least the features of an insulating film that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film, wherein the insulating film is formed to have a laminated-layer structure, as recited in present independent claims 1, 3, 13, and 15. Furthermore, Applicants also contend that neither *Wei*, *Mori*, nor *Sasaki*, taken either alone or in combination, anticipate or render obvious at least the features of an insulating film having a thickness of 100 nm or more that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film, wherein the insulating film is formed to have a laminated-layer structure, as recited in present independent claims 2 and 14.

As seen on pages 2 and 6 of the Office Action, the Examiner correctly admits that *Wei* fails to teach or disclose the feature of the insulating film having a laminated-layer structure, and is reliant on *Mori* for disclosing this feature.

Specifically, the Examiner purports that "Mori shows (fig. 10) a semiconductor device comprising a gate electrode (112) formed on a substrate and a gate insulating film (120) formed on the gate electrode", and that "[t]he gate insulating film has a laminated structure of three films (120a, 120b, and 120c) to provide an insulating film structure having a total breakdown voltage that is sufficiently high (col. 18, lines 25-43)" (see the Office Action, e.g., pages 2-3 and 6). However, lines 25-43 in column 18 of *Mori* actually state:

> Since in the embodiment, the **gate insulating films 120a and 120c**, interlayer insulating film 118, and protective insulating film 119 are formed in the temperature ranging of 250° to 270 ° C., the gate electrode 112 and scanning signal line 104 may be made of titanium-containing aluminum with a titanium content of 2.2% or more by weight. In the embodiment, the gate insulating film 120 is composed of a three-layer film consisting of **a lower SiN gate insulating film 120a, middle TaO_x gate insulating film 120b, and upper SiN gate insulating film 120c**, the middle gate insulating film 120b being a close insulating film made of a highly insulating metal oxide. Therefore, even if the upper and lower gate insulating films 120a, 120c are films with low breakdown voltages which have been made in the temperature ranging of 250° to 270° C. with the RF discharging power density range of 120 to 130 mW/cm^2, the total breakdown voltage of the three-layer film composed of the **gate insulating films 120a, 120b, and 120c** is sufficiently high.

As seen in the above passage, *Mori* merely discloses "a three-layer film consisting of a lower SiN *gate insulating film 120a*, middle TaO_x *gate insulating film 120b*, and upper SiN *gate insulating film 120c*." Although *Mori* may disclose a three layer gate insulating film, this layered film is actually formed under semiconductor layer 114, as seen in the copy of FIG. 10 provided below. In contrast, the insulating film of the present invention is not a layered gate insulating film as in *Mori*, but rather an insulating film that is interposed between a pair of n-type impurity regions.

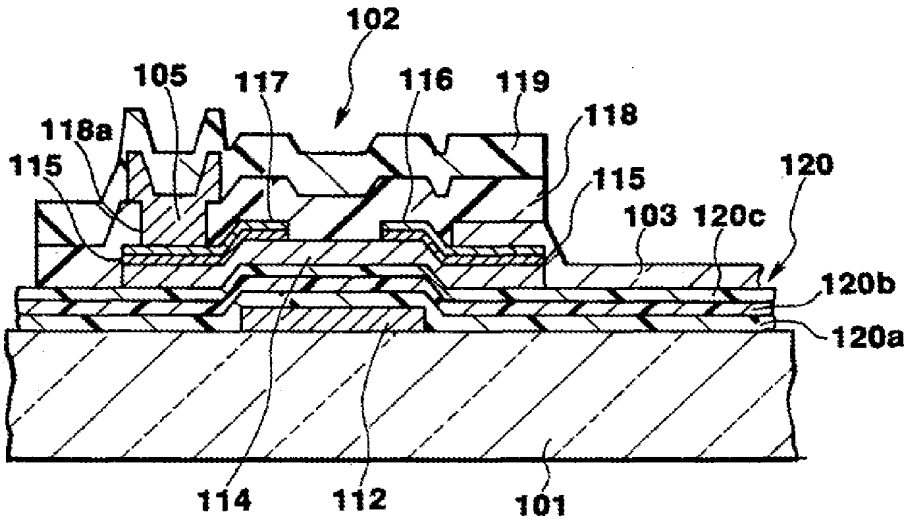

FIG.10

Furthermore, as seen above in FIG. 10, the three layer gate insulating film 120a, 120b, 120c of *Mori*, is NOT interposed between the pair of n-type impurity regions and that is formed over the semiconductor film, as in the present invention. Thus, the three layer gate insulating film described in *Mori* is unrelated to the insulating film that is interposed between a pair of n-type impurity regions of the present invention.

Moreover, *Sasaki* fails to remedy the deficiencies delineated above with respect to *Wei* and *Mori*. Consequently, neither *Wei*, *Mori*, nor *Sasaki*, taken either alone or in combination, anticipate or render obvious each and every feature recited in present independent claims 1-3 and 13-15.

Thus, the Examiner has failed to provide a proper *prima facie* case of obviousness in the rejection of present independent claims 1-3 and 13-15, and Applicants respectfully request that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn. Thus,

Applicants contend that independent claims 1-3 and 13-15 are in condition for allowance, and such action is hereby solicited.

Claims 4-6 and 16-18 are allowable at least by virtue of their dependency from one of the independent claims, but also because they are distinguishable over the prior art. Accordingly, Applicants respectfully request the withdrawal of the rejection, and the allowance of these claims.

In view of the foregoing, it is submitted that the present application is in condition for allowance and a notice to that effect is respectfully requested. If, however, the Examiner deems that any issue remains after considering this response, the Examiner is invited to contact the undersigned attorney to expedite the prosecution and engage in a joint effort to work out a mutually satisfactory solution.

Except for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 50-3557. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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